cell area with one of the source and drain of the second cell area, wherein the connecting area has an electric resistance which is lower than any one of the sources and drains of the first and second cell areas.

15. (amended) The semiconductor device according to claim 13, wherein an impurity concentration of the connecting area is the same as an impurity concentration of one of the sources and drains of the first and second cell areas, and is higher than an impurity concentration of the other of the sources and drains of the first and second cell areas.

16. (amended) The semiconductor device according to claim 13, wherein the impurity concentration of the connecting area is higher than the impurity concentrations of all the sources and drains of the first and second cell areas.

30. (amended) A semiconductor device comprising:

a semiconductor substrate including first and second memory cell areas;

the first memory cell area including a first horizontal field effect transistor comprising a first tunnel insulating film in contact with the semiconductor substrate, a first floating gate in contact with the first tunnel insulating film, a first dielectric layer in contact with the first floating gate, a first control gate in contact with the first dielectric layer, and first source/drain regions extending into the semiconductor substrate;

the second memory cell area including a second horizontal field effect transistor comprising a second tunnel insulating film in contact with the semiconductor substrate, a second floating gate in contact with the second tunnel insulating film, a second dielectric layer in contact with the second floating gate, a second control gate in contact with the second dielectric layer, and second source/drain regions extending into the semiconductor substrate;

the first source/drain regions and the second source/drain regions each including an upper surface that extends along a common plane;

a groove located in the semiconductor substrate at a position between the first and second memory cell areas; and

a connecting area capable of electrically connecting one of the first source/drain regions with one of the second source/drain regions, wherein the connecting area has an electric resistance which is lower than any of the source/drain regions, wherein the connecting area extends under the groove in the semiconductor substrate.

33. (amended) A semiconductor device comprising:

a semiconductor substrate including first and second memory cell areas;

the first memory cell area including a first field effect transistor comprising a first tunnel insulating film in contact with the substrate, a first floating gate in contact with the tunnel insulating film, a first dielectric layer in contact with the floating gate, a first control gate in contact with the dielectric layer, and first source/drain regions extending into the substrate;

the second memory cell area including a second field effect transistor comprising a second tunnel insulating film in contact with the substrate, a second floating gate in contact with the second tunnel insulating film, a second dielectric layer in contact with the second floating gate, a second control gate in contact with the second dielectric layer, and second source/drain regions extending into the substrate;

a connecting area capable of electrically connecting one of the first source/drain regions with one of the second source/drain regions, wherein the connecting area has an electric resistance which is lower than that of the first source/drain regions and lower than that of the second source/drain regions, and wherein the impurity concentration of the connecting area is higher than the impurity concentrations of the first source/drain regions and higher than the impurity concentrations of the second source/drain regions; and

a groove in the substrate above at least a portion of the connecting area, wherein no portion of the floating gate is positioned within the groove.

Please add new claims 34-39 as follows:

--34. (new) The semiconductor device according to claim 13, wherein the groove has a depth, and at least part of the connecting area has an impurity depth that is offset from that of that of the adjacent source/drain areas by the depth of the groove.

35. (new) A semiconductor device comprising:

first and second field effect transistors spaced apart from each other, each having source/drain regions in a semiconductor substrate;

a groove extending into the semiconductor substrate at a position between the first and second field effect transistors; and

a conducting region connecting a source/drain of the first field effect transistor to a source/drain of the second field effect transistor, the conducting region being positioned below the groove and the conducting region having a lower resistance than at least one of the source/drain regions.

36. (new) A semiconductor device according to claim 35, wherein the conducting region has a lower resistance than any of the source/drain regions.

37. (new). A semiconductor device according to claim 36, wherein the groove has a depth, and at least part of the connecting area has an impurity depth that is offset from that of that of the adjacent source/drain areas by the depth of the groove.

38. (new) A semiconductor device according to claim 35, further comprising an insulating material in contact with the semiconductor substrate in the groove.

39. (new) A semiconductor device comprising:

first and second memory cell means for storing data, the first and second memory cell means including source/drain regions formed in a semiconductor substrate;

a groove extending into the semiconductor substrate at a position between the first and second memory cell means; and

connecting means positioned under the groove for electrically connecting the first and second memory cell means, the connecting means having a resistance lower than that of the source/drain regions.--